PATENT ABSTRACTS OF JAPAN

(11)Publication number : 06-261337
(43)Date of publication of application : 16.09.1994

(51)Int.Cl. H04N 9/78

(21)Application number : 05-044213
(22)Date of filing : 05.03.1993

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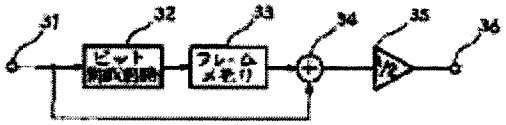
(54) DIGITAL SIGNAL PROCESSING CIRCUIT AND INTER-FRAME ARITHMETIC CIRCUIT

(57)Abstract:
PURPOSE: To reduce the storage capacity of a memory for obtaining a frame delay signal by storing a digital signal whose lower bit is eliminated.
CONSTITUTION: A decoding television signal converted into the digital signal is supplied to a bit elimination circuit 32 and an adder 34 through an input terminal 31. The bit elimination circuit 32 eliminates the lowest bit of a signal quantized by eight quantization bits, for example, and outputs highest seven bits to a frame memory 33. The frame memory 33 delays the decoding television signal of seven bits by one frame period and outputs it to an adder 34. The adder 34 adds the signal of eight bits at present time, which is inputted from the input terminal 31, with the output of the frame memory 33 being the signal of highest seven bits, which is prior by one frame period, by corresponding bits, and outputs an obtained two-fold Y signal to a coefficient unit 35. The coefficient unit 35 decreases the Y signal inputted from the adder 34 by 1/2, and outputs it to a mixer through an output terminal 36 as a still picture Y signal.



JAPANESE [JP,06-261337,A]

CLAIMS DETAILED DESCRIPTION TECHNICAL FIELD PRIOR ART EFFECT OF THE INVENTION TECHNICAL PROBLEM MEANS OPERATION EXAMPLE DESCRIPTION OF DRAWINGS DRAWINGS

[Translation done.]

* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1]A digital signal processing circuit comprising:
An input edge into which a digital signal of quantifying bit number M (M> 1) is inputted.
A memory measure in which predetermined carries out period memory except for at least 1 bit belonging to the low rank side of said digital signal.
A calculating means adding said digital signal and an output of said memory measure (or subtraction).

[Claim 2]An inter-frame arithmetic circuit comprising:
An input edge into which a television signal is inputted.
An A/D converter which changes said television signal into a digital signal by quantifying bit number M (M> 1), and outputs a digital television signal.
A memory measure in which predetermined carries out period memory except for 1 bit of said digital television signal which belongs to the low rank side at least.
A calculating means adding said digital television signal and an output of said memory measure (or subtraction).

[Claim 3]The inter-frame arithmetic circuit according to claim 2, wherein predetermined carries out period memory of said memory measure only except for a least significant bit.
[Claim 4]The inter-frame arithmetic circuit according to claim 2 or 3, wherein an integral multiple of one horizontal scanning period or 1 field period carries out period memory of said memory measure.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application]This invention relates to the digital signal processing circuit and inter-frame arithmetic circuit which subtract and add the predetermined digital signal which carried out period delay, and the digital signal before delay.
[0002]
[Description of the Prior Art]In recent years, the television receiver which changes a television signal into a digital signal and performs digital signal processing is developed. Thus, by changing a television signal into a digital signal and carrying out digital signal processing, three-dimensional Y/C separation using a digital memory can be performed, and highly precise Y/C separation characteristics can be acquired. Such an example of the conventional digital Y/C part ****** is explained below, referring to drawing 3 from drawing 2.
[0003]Drawing 2 is a figure showing the composition of the conventional digital Y/C part ******. In drawing 2, a decoding television signal is supplied to A/D converter 2 via the input edge 1. A/D converter 2 changes the inputted decoding television signal into a digital signal, and outputs it to the inter-frame Y/C eliminator 3, the Y/C eliminator 4 in the field, the motion detector 5, and the subtractor 7.
[0004]By carrying out frame addition with the decoding television signal before [one] having memorized inside, the inter-frame Y/C eliminator 3 extracts the static picture Y signal which is a Y signal used at the time of a static picture, and outputs it to the mixer 6. By adding with the decoding television signal of around one line memorized inside, the Y/C eliminator 4 in the field extracts the animation Y signal which is a Y signal used at the time of an animation, and outputs it to the mixer 6. By the method currently generally performed conventionally, the motion detector 5 detects a motion of the inputted decoding television signal, and outputs the motion detection signal according to this motion to the mixer 6.
[0005]The mixer 6 mixes the animation Y signal and static picture Y signal which were inputted by the ratio according to a motion detection signal, and outputs this mixed Y signal to the subtractor 7 and D/A converter 10 as a Y signal which carried out three-dimensional Y/C separation. This mixer 6 makes the ratio of an animation high, when it is shown that a motion of a decoding television signal is large, and when a small thing is shown, it makes the ratio of a static picture high.
[0006]The subtractor 7 subtracts the Y signal which is an output of the mixer 6 and which carried out three-dimensional Y/C separation from the digitized decoding television signal, and outputs it to the color demodulation circuit 8 as a C signal which carried out three-dimensional Y/C separation. The color demodulation circuit 8 restores to inputted C signal, and outputs it to D/A converter 9. D/A converter 9 changes into an analog signal this C signal to which it restored, and outputs it to the outgoing end 11. D/A converter 10 changes into an analog signal the Y signal which is an output signal of the mixer 6 and which carried out three-dimensional Y/C separation, and outputs it to the

outgoing end 12.
[0007]Next, the inter-frame Y/C eliminator 3 of drawing 2 is explained still in detail using drawing 3. In drawing 3, the output of A/D converter 2 is supplied to the frame memory 22 and the adding machine 23 via the input edge 21. The frame memory 22 is a memory which can memorize the decoding television signal by which it was digital-signal-ized for one frame, delays one frame period of inputted decoding television signals, and outputs them to the adding machine 23. The adding machine 23 outputs the Y signal of the twice as many size obtained by adding the output of the frame memory 22 which are the decoding television signal at present inputted from the input edge 21, and a decoding television signal in front of 1 frame period as this to the coefficient unit 24. The coefficient unit 24 doubles 1/of Y signals of a twice as many size as this inputted from the adding machine 23, and outputs them to the mixer 6 via the outgoing end 25 as a static picture Y signal.
[0008]The capacity of this frame memory 22 will be 525 line x910 pixel x8 bit =3,822,000 bit, when the quantized bit of the digital signal outputted from A/D converter 2 is 8 bits. about [thus,] -- since the memory of 4M bit was needed, there was a problem that circuit structure will become large.
[0009]
[Problem to be solved by the invention]Thus, in the conventional three-dimensional Y/C separation circuits, in order to acquire a frame delay signal, at least about four M a bit of a memory was needed, and there was a problem that circuit structure will become large. This invention removes the fault of the above conventional technologies, and it aims at reducing the memories for acquiring a frame delay signal.
[0010]
[Means for solving problem]In this invention in order to attain the above-mentioned purpose, The input edge into which the digital signal of quantifying bit number M (M> 1) is inputted, The digital signal processing circuit having a calculating means adding the output of the predetermined memory measure which carries out period memory, said digital signal, and said memory measure (or subtraction) except for at least 1 bit belonging to the low rank side of said digital signal is provided.
[0011]The input edge into which a television signal is inputted and the A/D converter which changes said television signal into a digital signal by quantifying bit number M (M> 1), and outputs a digital television signal, The inter-frame arithmetic circuit having a calculating means adding the output of the predetermined memory measure which carries out period memory, said digital television signal, and said memory measure (or subtraction) except for 1 bit of said digital television signal which belongs to the low rank side at least is provided. Said memory measure provides said inter-frame arithmetic circuit characterized by the predetermined thing to do for period memory only except for a least significant bit. Said memory measure provides said inter-frame arithmetic circuit characterized by the thing of the integral multiple of one horizontal scanning period or 1 field period to do for period memory.
[0012]
[Function]In what was constituted in this way, the digital signal of quantifying bit number M (M> 1) is inputted into an input edge. a memory measure removes 1 bit of said digital signal which belongs to the low rank side at least -- predetermined period memory -- it carries out. Since a calculating means adds and outputs the digital signal and the output of a memory measure which were supplied to the input edge, the storage capacity of a memory measure is reducible.
[0013]In what was constituted in this way, a television signal is inputted into an input edge and this television signal is changed into a digital television signal by the A/D converter. This digital television signal is memorized except for 1 bit which belongs to the low rank side at least by a memory measure. As for the output of this memory measure, and the output of an A/D converter, the operation of addition or subtraction is performed by the calculating means.
[0014]
[Working example]Hereafter, the working example of this invention is described in detail with

reference to drawing 1 and drawing 2. The composition of the three-dimensional Y/C separation circuits of this working example is the same as drawing 2.
[0015]Drawing 1 is a figure showing the composition which used the digital signal processing circuit concerning one working example of this invention for the inter-frame Y/C separation circuits 3 of drawing 2. It is explained that the quantized bit of this decoding television signal by which digital conversion was carried out is 8 bits.
[0016]In drawing 1, the decoding television signal changed into the digital signal is supplied to the bit cutback circuit 32 and the adding machine 34 via the input edge 31. The bit cutback circuit 32 deletes the least significant bit of the signal quantized by 8 bits of quantized bits, and outputs top 7 bits to the frame memory 33. The frame memory 33 delays one frame period of 7-bit decoding television signals, and outputs them to the adding machine 34. The adding machine 34 outputs the Y signal of the twice [about] as many size obtained by adding the output of the frame memory 33 which are the 8 bits decoding television signal at present inputted from the input edge 31, and top 7-bit decoding television signal in front of 1 frame period in corresponding bits as this to the coefficient unit 35. The coefficient unit 35 doubles 1/of Y signals of a twice [about] as many size as this inputted from the adding machine 34, and outputs them to the mixer 6 via the outgoing end 36 as a static picture Y signal.
[0017]Since least significant bits are reduced, the error of only the part of a least significant bit has produced the output of the frame memory 33 of this working example at the maximum. However, since frame addition is performing 8 bits and addition containing a least significant bit, the error turns into an error of the half of a least significant bit. Since there will almost be no influence in image quality if it is an error of this level, it is satisfactory.
[0018]Since the bit outputted from the bit cutback circuit 32 is top 7 bits, the capacity of this frame memory 33 will be 525 line x910 pixel x7 bit = 3,344,250 bit, and can be reduced to seven eighths. Thereby, degradation of image quality can make circuit structure of a memory there be nothing small.
[0019]In this working example, although the bit cutback circuit 32 reduced only least significant bits, if image quality may deteriorate for a while, it may reduce not only a least significant bit but both least significant bits and the bits of this one higher rank, and also may reduce it.
[0020]Although applied to the inter-frame Y/C eliminator 3 in this working example, it may apply to the memory which memorizes the decoding television signal of around one line in the Y/C eliminator 4 in the field. Although used for the Y/C eliminator in this working example, it may use for the noise rejection machine which performs addition and subtraction with the signal predetermined [, such as inter-frame,] which carried out period delay.
[0021]
[Effect of the Invention]The digital signal which deleted the lower bit of the digital signal in this invention according to invention.
Therefore, it is ****** about the capacity of the memory used for delay since it is carrying out.

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EXAMPLE

[Working example]Hereafter, the working example of this invention is described in detail with reference to drawing 1 and drawing 2. The composition of the three-dimensional Y/C separation circuits of this working example is the same as drawing 2.
[0015]Drawing 1 is a figure showing the composition which used the digital signal processing circuit concerning one working example of this invention for the inter-frame Y/C separation circuits 3 of drawing 2. It is explained that the quantized bit of this decoding television signal by which digital conversion was carried out is 8 bits.
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[0018]Since the bit outputted from the bit cutback circuit 32 is top 7 bits, the capacity of this frame memory 33 will be 525 line x910 pixel x7 bit = 3,344,250 bit, and can be reduced to seven eighths. Thereby, degradation of image quality can make circuit structure of a memory there be nothing small.
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[0020]Although applied to the inter-frame Y/C eliminator 3 in this working example, it may apply to the memory which memorizes the decoding television signal of around one line in the Y/C eliminator 4 in the field. Although used for the Y/C eliminator in this working example, it may use for the noise rejection machine which performs addition and subtraction with the signal predetermined [, such as inter-frame,] which carried out period delay.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]It is a figure showing the composition of one working example of the digital signal processing circuit concerning this invention.
[Drawing 2]It is a figure showing the composition of the digital Y/C separation circuits concerning the former and this invention.
[Drawing 3]It is a figure showing the composition of the conventional inter-frame Y/C separation eliminator.
[Explanations of letters or numerals]
31 [-- An adding machine, 35 / -- A coefficient unit, 36 / -- Outgoing end.] -- An input edge, 32 -- A bit cutback circuit, 33 -- A frame memory, 34

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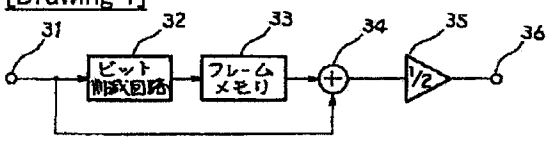
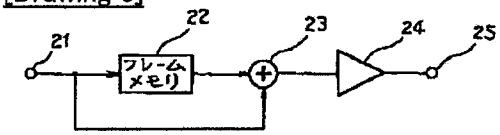
DRAWINGS

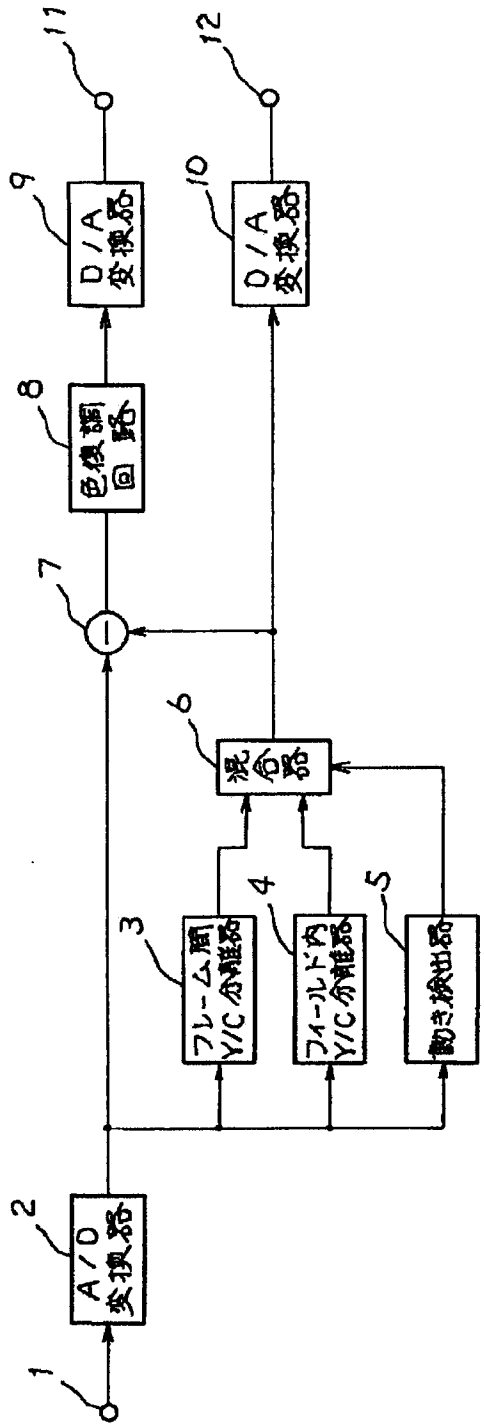
[Drawing 1]



[Drawing 3]



[Drawing 2]



[Translation done.]

(19)日本国特許庁（ＪＰ）　(12)公開特許公報（Ａ）　(11)特許出願公開番号
特開平6－261337
(43)公開日　平成６年(1994)９月16日

(51)Int.Cl.[5]	識別記号	庁内整理番号	Ｆ Ｉ	技術表示箇所
Ｈ０４Ｎ　9/78		Ａ　8626－5Ｃ		

審査請求　未請求　請求項の数４　ＯＬ　（全　５　頁）

(21)出願番号　特願平5－44213

(22)出願日　平成５年(1993)３月５日

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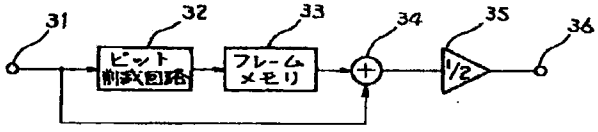
(54)【発明の名称】　デジタル信号処理回路、フレーム間演算回路

(57)【要約】
【目的】テレビジョン信号の遅延に用いるメモリの記憶容量を削減する。
【構成】デジタルテレビジョン信号は入力端３１を介してビット削減回路３２へ供給される。この信号はビット削減回路３２により最下位ビットが削減された後、フレームメモリ３３で１フレーム期間遅延される。この遅延された信号と入力端３１からの信号は加算器３４により加算され係数器３５へ出力される。係数器３５は加算器３４の出力を１／２倍して出力端３６へ出力する。



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【特許請求の範囲】

【請求項１】　量子化ビット数Ｍ（Ｍ＞１）のデジタル信号が入力される入力端と、

前記デジタル信号の下位側に属する少なくとも１ビットを除いて所定の期間記憶する記憶手段と、

前記デジタル信号と前記記憶手段の出力とを加算（または減算）する演算手段とを備えたことを特徴とするデジタル信号処理回路。

【請求項２】　テレビジョン信号が入力される入力端と、

前記テレビジョン信号を量子化ビット数Ｍ（Ｍ＞１）でデジタル信号に変換し、デジタルテレビジョン信号を出力するＡ／Ｄ変換器と、

前記デジタルテレビジョン信号の少なくとも下位側に属する１ビットを除いて所定の期間記憶する記憶手段と、

前記デジタルテレビジョン信号と前記記憶手段の出力とを加算（または減算）する演算手段とを備えたことを特徴とするフレーム間演算回路。

【請求項３】　前記記憶手段は、最下位ビットのみを除いて所定の期間記憶することを特徴とする請求項２記載のフレーム間演算回路。

【請求項４】　前記記憶手段は、１水平走査期間または１フィールド期間の整数倍の期間記憶することを特徴とする請求項２または３記載のフレーム間演算回路。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】この発明は、所定の期間遅延させたデジタル信号と遅延前のデジタル信号とを加減算するデジタル信号処理回路、フレーム間演算回路に関する。

【０００２】

【従来の技術】近年、テレビジョン信号をデジタル信号に変換してデジタル信号処理を行うテレビジョン受像機が開発されている。このようにテレビジョン信号をデジタル信号に変換してデジタル信号処理することにより、デジタルメモリを用いた３次元Ｙ／Ｃ分離が行え、高精度のＹ／Ｃ分離特性を得ることが出来る。以下にこのような従来のデジタルＹ／Ｃ分理回路の例を、図２から図３を参照しながら説明する。

【０００３】図２は従来のデジタルＹ／Ｃ分理回路の構成を示す図である。図２において、復号テレビジョン信号は、入力端１を介してＡ／Ｄ変換器２へ供給される。Ａ／Ｄ変換器２は、入力された復号テレビジョン信号をデジタル信号に変換し、フレーム間Ｙ／Ｃ分離器３，フィールド内Ｙ／Ｃ分離器４，動き検出器５および減算器７へ出力する。

【０００４】フレーム間Ｙ／Ｃ分離器３は、内部に記憶していた１フレーム前の復号テレビジョン信号とフレーム加算することにより静画時に用いるＹ信号である静画Ｙ信号を抽出し、混合器６へ出力する。フィールド内Ｙ／Ｃ分離器４は、内部に記憶していた１ライン前後の復

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号テレビジョン信号と加算することにより動画時に用いるＹ信号である動画Ｙ信号を抽出し、混合器６へ出力する。動き検出器５は従来一般に行われている方法により、入力された復号テレビジョン信号の動きを検出し、この動きに応じた動き検出信号を混合器６へ出力する。

【０００５】混合器６は、入力された動画Ｙ信号および静画Ｙ信号を、動き検出信号に応じた比率で混合し、この混合したＹ信号は３次元Ｙ／Ｃ分離したＹ信号として減算器７およびＤ／Ａ変換器１０へ出力する。この混合器６は復号テレビジョン信号の動きが大きいことを示すとき動画の比率を高くし、小さいことを示すとき静画の比率を高くする。

【０００６】減算器７は、デジタル化された復号テレビジョン信号から、混合器６の出力である３次元Ｙ／Ｃ分離したＹ信号を減算し、３次元Ｙ／Ｃ分離したＣ信号として色復調回路８へ出力する。色復調回路８は、入力されたＣ信号を復調しＤ／Ａ変換器９へ出力する。Ｄ／Ａ変換器９は、この復調されたＣ信号をアナログ信号へ変換し出力端１１へ出力する。Ｄ／Ａ変換器１０は、混合器６の出力信号である３次元Ｙ／Ｃ分離したＹ信号をアナログ信号へ変換し出力端１２へ出力する。

【０００７】次に、図２のフレーム間Ｙ／Ｃ分離器３について、図３を用いて更に詳細に説明する。図３において、Ａ／Ｄ変換器２の出力は入力端２１を介してフレームメモリ２２および加算器２３へ供給される。フレームメモリ２２は１フレーム分のデジタル信号化された復号テレビジョン信号を記憶することができるメモリであり、入力された復号テレビジョン信号を１フレーム期間遅延させ加算器２３へ出力する。加算器２３は、入力端２１から入力された現時点の復号テレビジョン信号と１フレーム期間前の復号テレビジョン信号であるフレームメモリ２２の出力とを加算し、得られた２倍の大きさのＹ信号を係数器２４へ出力する。係数器２４は、加算器２３から入力された２倍の大きさのＹ信号を１／２倍し、静画Ｙ信号として出力端２５を介して混合器６へ出力する。

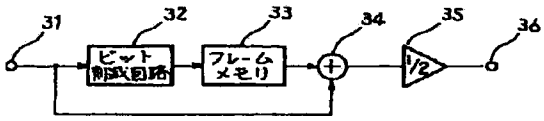
【０００８】このフレームメモリ２２の容量は、Ａ／Ｄ変換器２から出力されるデジタル信号の量子化ビットが８ビットであるとき５２５ライン×９１０画素×８ビット＝3,822,000ビットとなる。このように約４Ｍビットのメモリを必要とするので、回路規模が大きくなってしまうという問題があった。

【０００９】

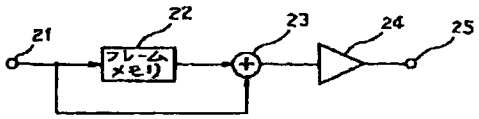
【発明が解決しようとする課題】このように従来の３次元Ｙ／Ｃ分離回路においては、フレーム遅延信号を得る為に少なくとも約４Ｍビットのメモリを必要とし、回路規模が大きくなってしまうという問題があった。この発明は上記のような従来技術の欠点を除去し、フレーム遅延信号を得るためのメモリを削減することを目的とするものである。

【００１０】
【課題を解決するための手段】上記の目的を達成するために、この発明においては、量子化ビット数M（M＞１）のデジタル信号が入力される入力端と、前記デジタル信号の下位側に属する少なくとも１ビットを除いて所定の期間記憶する記憶手段と、前記デジタル信号と前記記憶手段の出力とを加算（または減算）する演算手段とを備えたことを特徴とするデジタル信号処理回路を提供する。
【００１１】また、テレビジョン信号が入力される入力端と、前記テレビジョン信号を量子化ビット数M（M＞１）でデジタル信号に変換し、デジタルテレビジョン信号を出力するA／D変換器と、前記デジタルテレビジョン信号の少なくとも下位側に属する１ビットを除いて所定の期間記憶する記憶手段と、前記デジタルテレビジョン信号と前記記憶手段の出力とを加算（または減算）する演算手段とを備えたことを特徴とするフレーム間演算回路を提供する。また、前記記憶手段は、最下位ビットのみを除いて所定の期間記憶することを特徴とする前記フレーム間演算回路を提供する。また、前記記憶手段は、１水平走査期間または１フィールド期間の整数倍の期間記憶することを特徴とする前記フレーム間演算回路を提供する。
【００１２】
【作用】このように構成されたものにおいては、入力端に量子化ビット数M（M＞１）のデジタル信号が入力される。記憶手段は前記デジタル信号の少なくとも下位側に属する１ビットを除いて所定の期間記憶する。演算手段は入力端に供給されたデジタル信号と記憶手段の出力とを加算して出力するので、記憶手段の記憶容量を削減することができる。
【００１３】このように構成されたものにおいては、入力端にテレビジョン信号が入力され、このテレビジョン信号はA／D変換器によりデジタルテレビジョン信号に変換される。このデジタルテレビジョン信号は記憶手段により少なくとも下位側に属する１ビットを除いて記憶される。この記憶手段の出力とA／D変換器の出力とは演算手段により加算または減算の演算が行われる。
【００１４】
【実施例】以下、この発明の実施例について、図１および図２を参照して詳細に説明する。この実施例の３次元Y／C分離回路の構成は図２と同じである。
【００１５】図１はこの発明の一実施例に係るデジタル信号処理回路を、図２のフレーム間Y／C分離回路３に用いた構成を示す図である。このデジタル変換された復号テレビジョン信号の量子化ビットは８ビットであるとして説明する。
【００１６】図１において、デジタル信号に変換された復号テレビジョン信号は入力端３１を介してビット削減回路３２および加算器３４へ供給される。ビット削減回路３２は、量子化ビット８ビットで量子化された信号の最下位ビットを削除し、上位７ビットをフレームメモリ３３へ出力する。フレームメモリ３３は、７ビットの復号テレビジョン信号を１フレーム期間遅延させ加算器３４へ出力する。加算器３４は、入力端３１から入力された現時点の８ビットの復号テレビジョン信号と１フレーム期間前の上位７ビットの復号テレビジョン信号であるフレームメモリ３３の出力とを対応するビットどうしで加算し、得られた約２倍の大きさのY信号を係数器３５へ出力する。係数器３５は、加算器３４から入力された約２倍の大きさのY信号を１／２倍し、静画Y信号として出力端３６を介して混合器６へ出力する。
【００１７】この実施例のフレームメモリ３３の出力は最下位ビットが削減されているので、最大で最下位ビットの分だけの誤差が生じている。しかし、フレーム加算は最下位ビットを含む８ビットと加算を行っているので、その誤差は最下位ビットの半分の誤差となる。この程度の誤差ならば画質にほとんど影響がないので問題ない。
【００１８】このフレームメモリ３３の容量は、ビット削減回路３２から出力されるビットが上位７ビットであるので、５２５ライン×９１０画素×７ビット＝　３，３４４，２５０ビットとなり、７／８に削減することができる。これにより画質の劣化無くメモリの回路規模を小さくすることが出来る。
【００１９】また、この実施例ではビット削減回路３２は最下位ビットのみ削減したが、少し画質が劣化してもよいのなら最下位ビットだけでなく最下位ビットおよびこの１つ上位のビットの両方を削減しても良いし、更に削減しても良い。
【００２０】また、この実施例ではフレーム間Y／C分離器３へ適用したが、フィールド内Y／C分離器４内の１ライン前後の復号テレビジョン信号を記憶しておくメモリへ適用しても良い。また、この実施例ではY／C分離器に用いたが、フレーム間等所定の期間遅延させた信号との加減算を行うノイズ除去器に用いてもよい。
【００２１】
【発明の効果】この発明によれば、デジタル信号の下位ビットを削除したデジタル信号をメモリしているので、遅延に用いるメモリの容量を削減することができる。
【図面の簡単な説明】
【図１】この発明に係るデジタル信号処理回路の一実施例の構成を示す図である。
【図２】従来およびこの発明に係るデジタルY／C分離回路の構成を示す図である。
【図３】従来のフレーム間Y／C分離分離器の構成を示す図である。
【符号の説明】
３１…入力端、３２…ビット削減回路、３３…フレームメモリ、３４…加算器、３５…係数器、３６…出力端。

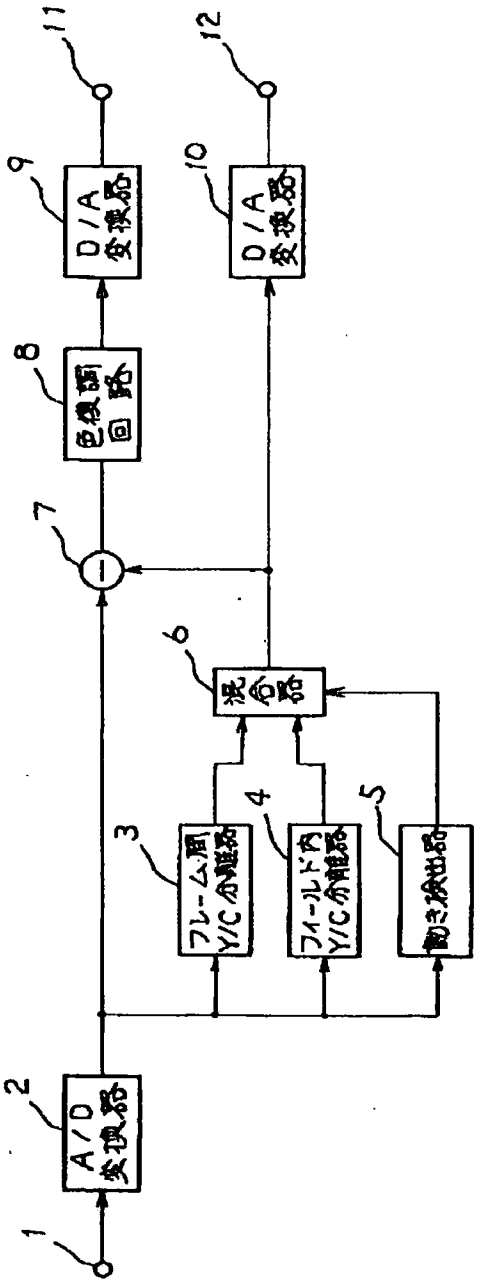
【図１】



【図３】



【図２】


11
12
9
D/A 変換器
10
D/A 変換器
8
色復調回路
7
6
混合器
3
フレーム間 Y/C 分離器
4
フィールド内 Y/C 分離器
5
動き検出器
2
A/D 変換器
1